CLAIMS

What is claimed is:

1. A process tolerant sensor apparatus comprising:

a) a bottom substrate;

b) a top substrate;

c) a plurality of sensors disposed between the bottom substrate and the top substrate;

d) a plurality of electrically conductive interconnects disposed between the bottom substrate and the top substrate;

e) electrically active components connected to the conductive interconnects for at least one of data acquisition, data storage, and communications; and

f) a bonding material substantially filling the volume between the bottom substrate and the top substrate.

2. The sensor apparatus of claim 1, wherein the bottom substrate comprises a silicon wafer.

3. The sensor apparatus of claim 1, wherein the top substrate comprises a silicon wafer.

4. The sensor apparatus of claim 1, wherein the top substrate comprises at least one of quartz and silica.

5. The sensor apparatus of claim 1, wherein the bonding material is configured as a layer having a thickness between 0.05 mm and 10 mm.

6. The sensor apparatus of claim 4, wherein the bonding material comprises at least one of following polymeric materials Silicone, Epoxy, Acrylic, Polyimide, Polyurethane, and Butyl rubber.

7. The sensor apparatus of claim 1, wherein the top substrate comprises an RF shielding material.

8. The sensor apparatus of claim 7, wherein the RF shielding material comprises at least one of:

a) an electrically conductive layer and

b) a magnetically permeable layer.

9. The sensor apparatus of claim 8, wherein the shielding material includes layers patterned so as to enhance the shielding efficiency over predetermined frequency ranges.

10. The sensor apparatus of claim 1, wherein at least one of the bottom substrate and the top substrate is thinned so that the thickness of the sensor apparatus substantially equals the thickness of a predetermined workpiece.

11. The sensor apparatus of claim 1, wherein:

the plurality of sensors and electrically conductive interconnects are disposed upon the surface of the bottom substrate,

a mirror image pattern of the sensors and interconnects is disposed upon the surface of the top substrate, and wherein the mirror image pattern and the sensors are of substantially the same thickness.

12. The sensor apparatus of claim 1, wherein at least one of the electrically active components is disposed upon the surface of the

bottom substrate, the top substrate has a hole, and the at least one of the electrically active components extends into the hole in the planar top substrate.

13. The sensor apparatus of claim 1, wherein the bottom substrate is electrically isolated from the top substrate.

14. The sensor apparatus of claim 1, wherein the bottom substrate is electrically connected to the top substrate.

15. The sensor apparatus of claim 7, wherein the RF shielding material comprises at least one of

a) an electrically conductive layer and

b) a magnetically permeable layer.

16. The sensor apparatus of claim 7, wherein the RF shielding material comprises at least one of

a) an electrically conductive layer comprising at least one of silver, nickel, aluminum, and carbon, and

b) a magnetically permeable film or layer comprising at least one of iron and cobalt.

17. The sensor apparatus of claim 1, wherein the bottom substrate is selected from the group consisting of semiconductor wafer substrate, lithography mask substrate, printed circuit board substrate, and flat panel display substrate and the top substrate is selected from the group consisting of semiconductor wafer substrate, lithography mask substrate, printed circuit board substrate, and flat panel display substrate.

18. In a combination:

a bottom semiconductor wafer;

a top semiconductor wafer;

a plurality of sensors disposed between the bottom semiconductor wafer and the top semiconductor wafer;

a plurality of electrically conductive interconnects disposed between the bottom semiconductor wafer and the top semiconductor wafer;

an electronics module comprising a housing containing electrically active components connected to the conductive interconnects for at least one of data acquisition, data storage, and communications; and

a bonding material substantially filling the volume between the bottom semiconductor wafer and the top semiconductor wafer.

19. The combination of claim 18 further comprising the top semiconductor wafer having a hole for receiving at least a portion of the electronics module.

20. The combination of claim 18 further comprising the top semiconductor wafer having a layer of electromagnetic field shielding material.